

- 1 What is claimed is:
- 2 1. A semiconductor build-up package comprising:
- 3 a die having an active surface , a passive surface, sides between the active surface and
- 4 the passive surface, and a plurality of bonding pads on the active surface of the die;
- 5 a metal carrier having a surface with a cavity for accommodating the die; and
- 6 a plurality of dielectric layers formed on the active surface of the die and the surface
- 7 of the metal carrier, wherein each dielectric layer has a plurality of conductive
- 8 columns for inner electrical connection of the bonding pads of the die, at least a layer
- 9 of conductive traces is formed between the dielectric layers.
- 10 2. The semiconductor build-up package in accordance with claim 1, wherein the surface
- 11 of the metal carrier is coplanar to the active surface of the die.
- 12 3. The semiconductor build-up package in accordance with claim 1, wherein at least one
- 13 conductive column of one of the dielectric layers is vertically bonded on the conductive
- 14 column of the adjacent dielectric layer.
- 15 4. The semiconductor build-up package in accordance with claim 1, further comprising
- 16 a plurality of solder balls, bumps or pins on the outermost dielectric layer.
- 17 5. The semiconductor build-up package in accordance with claim 4, wherein the
- 18 plurality of solder balls are in grid array fashion.
- 19 6. The semiconductor build-up package in accordance with claim 1, wherein the metal
- 20 carrier is made of copper, aluminum or their alloys.
- 21 7. The semiconductor build-up package in accordance with claim 1, wherein the
- 22 conductive columns are made of copper, aluminum or their alloys.
- 23 8. The semiconductor build-up package in accordance with claim 1, wherein the
- 24 dielectric layers are polyimide, epoxy, BT resin, FR-4 resin, FR-5 resin, BCB, or
- 25 PTFE.
- 26 9. The semiconductor build-up package in accordance with claim 1, wherein the metal
- 27 carrier covers the passive surface and the sides of the die.

- 1 10. A semiconductor build-up package comprising:
2 a die having an active surface , a passive surface and a plurality of bonding pads on
3 the active surface of the die;
4 a metal carrier having a surface with a cavity for accommodating the die; and
5 a first dielectric layer on the active surface of the die and the surface of the metal
6 carrier, wherein the first dielectric layer has a plurality of conductive columns bonded
7 on the bonding pads of the die.
- 8 11. The semiconductor build-up package in accordance with claim 10, wherein the
9 surface of the metal carrier is coplanar to the active surface of the die.
- 10 12. The semiconductor build-up package in accordance with claim 10, further comprising
11 at least a dielectric layer with conductive columns formed on the first dielectric layer.
- 12 13. The semiconductor build-up package in accordance with claim 12, further comprising
13 solder balls, bumps or pins are formed on the outermost dielectric layer.
- 14 14. The semiconductor build-up package in accordance with claim 10, wherein the metal
15 carrier is made of copper, aluminum or their alloys.
- 16 15. The semiconductor build-up package in accordance with claim 10, wherein the
17 conductive columns are made of copper, aluminum or their alloys.
- 18 16. The semiconductor build-up package in accordance with claim 10, wherein the
19 plurality of dielectric layers are polyimide, epoxy, BT resin, FR-4 resin, FR-5 resin,
20 BCB, or PTFE.
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